UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,975	11/20/2003	Ha Chu Vu	08211/0200375-US0/P05816	2727

38845 7590 09/21/2006

DARBY & DARBY P.C.
P.O. BOX 5257
NEW YORK, NY 10150-5257

EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,975	VU, HA CHU	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed the 25 August 2006. Claims 1-20 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. (US 2004/0032406) in view of Donnelly et al. (US 2004/0223571) and further in view of Agazzi (US 2002/0122503).

Regarding claim 1, Agarwal et al. disclose an interface circuit for processing an analog color signal comprising:

a phase locked loop (PLL) circuit adapted to generate a plurality of phased signals from a synchronizing signal that is associated with the analog color signal (Figure 4, item 416 and paragraph [0027] explain that PLL can perform frequency synthesis on the HSYNC signal.);

a phase adjuster adapted to generate an adjustable delay signal (Figure 4, item 406 and paragraph [0027] explain that the delay generator can introduce inter-pixel phase delays in equal intervals.); and

an analog to digital converter adapted to improve processing of the analog color signal (Figure 4 shows digitizer 402 which contains ADCs 411, 412 and 414 as explained in paragraph [0027].).

Agarwal et al. fail to disclose of the phase adjuster adapted to generate an adjustable delay signal from two of the plurality of phased signals that are apart from each other by an odd multiple of approximately 45 degrees, and choosing the adjustment to the delay signal, wherein at least one simulated phase is provided.

Donnelly et al. disclose of a phase adjuster which is adapted to generate an adjustable delay signal from two of a plurality of phased signals that are apart from each other by an odd multiple of approximately 45 degrees (Paragraph [0036] and Figure 12 explain that the DLL 100 shown in Figure 1 generates phase vectors spaced at 45 degree intervals. Then in combination with the circuit shown in Figure 6, circuit 500 is able to generate the delay signal output clk 640 from two of the vectors which are spaced 45 degrees apart.) and

choosing the adjustment to the delay signal, wherein at least one simulated phase is provided (Paragraph [0036] and Figure 12 explains that the DLL generates simulated phase vectors spaced apart by 45 degrees. Then paragraph [0053] explains that two vectors Kx and Ky are chosen from the simulated phases, where the chosen vectors are used by the adjustable delay section 610 shown in Figure 6 to create the adjustable delay.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the phase adjuster taught by Donnelly et al. to replace the phase adjuster taught by Agarwal et al. in order to provide a method and circuitry to generate a set of phase vectors in a way that is more immune to noise on loop inputs including power supplies, leading to a more stable set of phase vectors.

Agarwal et al. and Donnelly et al. fail to teach of choosing the adjustment for the delay signal to improve processing of the analog color signal.

Agazzi discloses that the operational parameters of an ADC may be adjusted, such as the delay, offset, gain, etc in order to ensure that the sampling of the ADC is

performed uniformly and with proper phase and time delays between samples to ensure that digital data is a true rendition of the analog data (Paragraph [0103]).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to make the ADC taught by the combination of Agarwal et al. and Donnelly et al. improve the processing of the analog color signal by choosing an adjustment to the delay signal as taught by Agazzi in order to ensure that digital data is a true rendition of the analog data.

Regarding claim 2, Agarwal et al., Donnelly et al. and Agazzi disclose the circuit of claim 1.

Agarwal et al. also disclose wherein the synchronizing signal is intended to generate a pixel clock in a display, and the phased signals replicate those of the pixel clock (Paragraph [0027] explains that the HSYNC corresponds to a pixel clock and that the signals output by the PLL set the pixel clock frequency.).

Regarding claim 3, Agarwal et al., Donnelly et al. and Agazzi disclose the circuit of claim 1.

Donnelly et al. also disclose wherein the phase adjuster includes:

a first phase selector for selecting a first one of the phased signals (Figure 6, selection circuitry 510 selects a first one of the phased signals K<r:0> Kx 520.);

a second phase selector for selecting a second one of the phased signals (Figure 6, selection circuitry 510 selects a first one of the phased signals K<r:0> Ky 530.); and

a phase mixer for multiplying the first selected phased signal with a first weight, multiplying the second selected phased signal with a second weight, and adding together the first and the second multiplied phased signals to derive the delay signal (Figure 6, phase interpolator 560 is explained in paragraphs [0055]- [0057], where the values of currents 1720 and 1730 are adjusted such that the combination of the two signals can create any delay.).

Regarding claim 4, Agarwal et al., Donnelly et al. and Agazzi disclose the circuit of claim 3.

Donnelly et al. also disclose wherein the phase adjuster further includes:

a decoder to generate phase selection signals for selecting the first and second phased signals (Figure 6 shows that control circuit 570 creates sel<s:0> to select the first and second phase signals as explained in paragraph [0057].).

Regarding claim 5, Agarwal et al., Donnelly et al. and Agazzi disclose the circuit of claim 4.

Donnelly et al. also disclose wherein some of the phase selection signals are received into the phase mixer (As explained above, the examiner interprets that the selection signals received by the selection circuitry 510 are received into the phase interpolator 560 via the selected signals Kx and Ky.).

Regarding claim 6, Agarwal et al., Donnelly et al. and Agazzi disclose the circuit of claim 3.

Donnelly et al. also disclose wherein the phase adjuster further includes:

a Phase Digital to Analog Converter for generating a first weight signal representing the first weight and a second weight signal representing the second weight, and wherein the phase mixer receives the first weight signal and the second weight signal to derive the delay signal (Figures 6 and 18 and paragraph [0056] explain that the currents 1720 and 1730 that are used to weight the signals must be received by the phase interpolator 560 in order to derive the delay signal stating that the phase interpolator functions as a weighted integrator. Paragraph [0057] explains that the phase interpolator is adjusted to produce an output.).

Regarding claim 7, Agarwal et al., Donnelly et al. and Agazzi disclose the circuit of claim 6.

Donnelly et al. also disclose wherein the phase adjuster further includes:

a decoder to generate weight selection signals for generating the first and second weight signals (Figure 6 shows that control circuit 570 create the signals applied to phase interpolator 560 for selecting the weighted signals.).

Regarding claim 8, Agarwal et al., Donnelly et al. and Agazzi disclose the circuit of claim 6.

Donnelly et al. also disclose wherein the first and second weights have a substantially constant sum total weight (Paragraph [0056] explains that the currents 1720 and 1730 are adjustable but that if one or the other is at maximum and minimum then the delay can be generator different ways meaning that the sum weight is substantially constant.).

Regarding claim 9, Agarwal et al., Donnelly et al. and Agazzi disclose the circuit of claim 8.

Donnelly et al. also disclose wherein the Phase Digital to Analog converter includes

a first current source drawing a first current that represents the first weight (Figure 18 and paragraph [0056] explain current source 1720 draws a first current.),

a second current source drawing a second current that represents the sum total weight (Figure 18 and paragraph [0056] explain that the coincidence detector 1860 draws currents from lines 1840 and 1850 to determine a total weight.), and

a third current source drawing a difference current between the second current and the first current, wherein the difference current is used to derive the second weight signal (Figure 18 and paragraph [0056] explain that current source 1730 draws a current which is the difference between a total current and the first current, which represents a second weight.).

Regarding claim 10, Agarwal et al., Donnelly et al. and Agazzi disclose the circuit of claim 8.

Donnelly et al. also disclose wherein the sum total weight equals a multiplication integer times four, and the first weight equals the multiplication integer times one of zero, one, two, three and four (Paragraph [0056] explains that the current source 1720 can be set to zero, meaning that during an adjustment period for a particular delay, if current source 1720 is zero, then the multiplication factor could be any number multiplied by zero which would obtain the total weight being a number times 4, i.e. the total sum divided by 4 would be the multiplication factor.).

Regarding claim 11, this claim is rejected under the same rationale as claim 1.

Regarding claim 12, please refer to the rejection of claim 1.

Regarding claim 13, this claim is rejected under the same rationale as claim 1.

Regarding claim 14, please refer to the rejection of claim 1.

Regarding claim 15, this claim is rejected under the same rationale as claim 2.

Regarding claim 16, Agarwal et al., Donnelly et al. and Agazzi disclose the method of claim 13.

Donnelly et al. also disclose wherein deriving is performed by:

determining the location of a general requested delay in a phase diagram (Figure 12 shows the phase diagram used to derive the delay.); and

selecting the two phased signals such that they define a sector between on the phase diagram that encompasses the general required delay (Figure 6 and paragraph [0057] explain that the pair of signals selected are chosen based on the required delay.).

Regarding claim 17, this claim is rejected under the same rationale as claim 3.

Regarding claim 18, Agarwal et al., Donnelly et al. and Agazzi disclose the method of claim 17.

Donnelly et al. also disclose the method further comprising:

selecting first and second weights so as to simulate the general requested delay within the sector (Paragraph [0056] explains that the weights are selected to generate the delay required.).

Regarding claim 19, this claim is rejected under the same rationale as claim 9.

Regarding claim 20, this claim is rejected under the same rationale as claim 10.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Morita (US 6,621,480) discloses of a phase adjuster for adjusting the phase of a picture signal based on the same number of clock pulses as that of picture elements in each horizontal line of the display screen.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

13 September 2006

AMR A. AWAD
SUPERVISORY PATENT EXAMINER